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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	MI22-1171
First Inventor or Application Identifier	Salman Akram
Title	Methods of Forming a Transistor Gate
Express Mail Label No.	EL369520905US

jc518 U.S. PTO 09/292132 04/14/99

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 27] Inc. Title Pg.
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 4]
4. Oath or Declaration [*Total Pages* 3]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [X] Other: Check; Change of Address

16. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08 / 993,663

Prior application information: *Examiner* S. Mulpuri *Group / Art Unit:* 2812

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Signature		*Date*	April 14, 1999

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/993,663
Priority Filing Date ..... December 18, 1997
Inventor ..... Salman Akram et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2812
Priority Examiner ..... S. Mulpuri
Attorney's Docket No. MI22-1171
Title: Methods of Forming a Transistor Gate (As Amended)

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: James D. Shaurette (Tel. 509-624-4276; Fax 509-838-3424)
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AMENDMENTS

In the Title

Please replace the title with --Methods of Forming a Transistor Gate--.

In the Specification

At p. 1, before the "Technical Field" section, insert

--**RELATED PATENT DATA**

This patent application is a continuation resulting from U.S. Patent Application Serial No. 08/993,663, which was an application filed on December 18, 1997.--

In the Claims

Cancel claims 1-50.

Add the following new claims 51-75.

51. A method of forming a transistor gate comprising:

forming a gate oxide layer over a semiconductive substrate;

providing at least one of fluorine or chlorine within the gate oxide layer; and

forming a gate proximate the gate oxide layer after the providing.

52. The method of claim 51 wherein the chlorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

53. The method of claim 51 wherein the gate comprises opposing lateral edges and a central region therebetween, the chlorine being provided within the gate oxide layer to a greater concentration proximate at least one of the gate edges than in the central region.

54. The method of claim 51 wherein the providing comprises providing fluorine.

55. A method of forming a transistor gate comprising:

forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a center therebetween, the gate oxide having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate; and

concentrating at least one of chlorine or fluorine in the gate oxide layer within the overlap more proximate at least one of the outwardly exposed oxide gate edges than the center.

56. The method of claim 55 wherein the concentrating comprises concentrating fluorine.

57. The method of claim 55 wherein the gate is formed to have a gate width between the edges of 0.25 micron or less, the concentrating forming at least one concentration region in the gate oxide which extends laterally inward from the at least one gate edge no more than about 500 Angstroms.

58. The method of claim 55 wherein the concentrating comprises diffusion doping.

59. The method of claim 55 wherein the concentrating comprises ion implanting.

60. The method of claim 55 wherein the removing comprises removing portions of the gate oxide layer not overlapping the gate.

61. The method of claim 55 wherein the concentrating follows the removing.

62. A method of forming a transistor gate comprising:

forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a central region therebetween;

forming sidewall spacers comprising at least one of the chlorine or fluorine proximate the opposing edges; and

doping the gate oxide layer within the overlap with at least one of chlorine or fluorine proximate the opposing gate edges and leaving the central region substantially undoped with chlorine and fluorine.

63. The method of claim 62 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

64. The method of claim 62 further comprising removing portions of the gate oxide layer not overlapping the gate.

65. The method of claim 62 wherein the doping comprises diffusion doping at least one of chlorine or fluorine from the spacers into the gate oxide layer.

66. The method of claim 65 further comprising annealing the spacers to provide the diffusion doping.

67. The method of claim 62 wherein the doping comprises doping with fluorine.

68. A method of forming a transistor gate comprising the following sequential steps:

forming a gate over a gate oxide layer, the gate having opposing lateral edges;

forming sidewall spacers comprising at least one of chlorine or fluorine proximate the opposing lateral edges; and

diffusion doping at least one of chlorine or fluorine into the gate oxide layer beneath the gate from laterally outward of the gate edges.

69. The method of claim 68 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

70. The method of claim 68 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms.

71. The method of claim 68 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms, the concentration regions having an average dopant concentration in the gate oxide layer proximate the edges from about 1 x 10^{19} atoms/cm^3 to about 1 x 10^{21} atoms/cm^3.

72. The method of claim 71 wherein the gate oxide layer between the concentration regions is substantially undoped with chlorine and fluorine.

73. The method of claim 68 further comprising removing portions of the gate oxide layer not beneath the gate.

74. The method of claim 68 wherein the diffusion doping comprises annealing the sidewall spacers.

75. The method of claim 68 wherein the diffusion doping comprises diffusion doping fluorine.

REMARKS

Claims 1-50 are canceled, and new claims 51-75 are added. Claims 51-75 are pending in the application, and Applicant requests examination of such pending claims.

Respectfully submitted,

Dated: April 14, 1999

By: ______________________

James D. Shaurette
Reg. No.: 39,833

EL156304819

EL369520905

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Semiconductor Processing Method And Field Effect Transistor

* * * * *

INVENTOR

Salman Akram
Akram Ditali

ATTORNEY'S DOCKET NO. MI22-695

SEMICONDUCTOR PROCESSING METHOD AND FIELD EFFECT TRANSISTOR

TECHNICAL FIELD

This invention relates to methods of forming transistor gates and to transistor constructions.

BACKGROUND OF THE INVENTION

As transistor gate dimensions are reduced and the supply voltage remains constant, the lateral field generated in MOS devices increases. As the electric field becomes strong enough, it gives rise to so-called "hot-carrier" effects in MOS devices. This has become a significant problem in NMOS devices with channel lengths smaller than 1.5 micron, and in PMOS devices with sub-micron channel lengths.

High electric fields cause the electrons in the channel to gain kinetic energy, with their energy distribution being shifted to a much higher value than that of electrons which are in thermal equilibrium within the lattice. The maximum electric field in a MOSFET device occurs near the drain during saturated operation, with the hot electrons thereby becoming hot near the drain edge of the channel. Such hot electrons can cause adverse effects in the device.

First, those electrons that acquire greater than or equal to 1.5 eV of energy can lose it via impact ionization, which generates electron-hole pairs. The total number of electron-hole pairs generated by impact

ionization is exponentially dependent on the reciprocal of the electric field. In the extreme, this electron-hole pair generation can lead to a form of avalanche breakdown. Second, the hot holes and electrons can overcome the potential energy barrier between the silicon and the silicon dioxide, thereby causing hot carriers to become injected into the gate oxide. Each of these events brings about its own set of repercussions.

Device performance degradation from hot electron effects have been in the past reduced by a number of techniques. One technique is to reduce the voltage applied to the device, and thus decrease in the electric field. Further, the time the device is under the voltage stress can be shortened, for example, by using a lower duty cycle and clocked logic. Further, the density of trapping sites in the gate oxide can be reduced through the use of special processing techniques. Also, the use of lightly doped drains and other drain engineering design techniques can be utilized.

Further, it has been recognized that fluorine-based oxides can improve hot-carrier immunity by lifetime orders of magnitude. This improvement is understood to mainly be due to the presence of fluorine at the Si/SiO_2 interface reducing the number of strained Si/O bonds, as fewer sites are available for defect formation. Improvements at the Si/SiO_2 interface reduces junction leakage, charge trapping and interface trap generation. However, optimizing the process can be complicated. In addition, electron-trapping and poor leakage characteristics can make

such fluorine-doped oxides undesirable and provide a degree of unpredictability in device operation. Use of fluorine across the entire channel length has been reported in, a) K. Ohyu et al., "Improvement of SiO_2/Si Interface Properties by Fluorine Implantation"; and b) P.J. Wright, et al., "The Effect of Fluorine On Gate Dielectric Properties".

SUMMARY OF THE INVENTION

In one implementation, a method of forming a transistor includes forming a gate oxide layer over a semiconductive substrate. Chlorine is provided within the gate oxide layer. A gate is formed proximate the gate oxide layer. In another aspect, a gate and a gate oxide layer are formed in overlapping relation, with the gate having opposing edges and a center therebetween. At least one of chlorine or fluorine is concentrated in the gate oxide layer within the overlap more proximate at least one of the gate edges than the center. The center is preferably substantially void of either fluorine of chlorine. In one implementation, at least one of chlorine or flouring is angle ion implanted to beneath the edges of the gate. In another, sidewall spacers are formed proximate the opposing lateral edges, with the sidewall spacers comprising at least one of chlorine or fluorine. The spacers are annealed at a temperature and for a time period effective to diffuse the fluorine or chlorine from the spacers into the gate oxide

layer to beneath the gate. Transistors fabricated by such methods, and other methods, are also contemplated.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a sectional view of a semiconductor wafer fragment in accordance with the invention.

Fig. 2 is a sectional view of an alternate semiconductor wafer fragment at one step of a method in accordance with the invention.

Fig. 3 is a view of the Fig. 2 wafer at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a sectional view of another semiconductor wafer fragment at an alternate processing step in accordance with the invention.

Fig. 5 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that depicted by Fig. 4.

Fig. 6 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that depicted by Fig. 5.

Fig. 7 is a view of the Fig. 4 wafer at an alternate processing step to that depicted by Fig. 6.

Fig. 8 is a sectional view of another semiconductor wafer fragment at another processing step in accordance with the invention.

Fig. 9 is a view of the Fig. 8 wafer at a processing step subsequent to that depicted by Fig. 8.

Fig. 10 is a sectional view of still another embodiment wafer fragment at a processing step in accordance with another aspect of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A semiconductor wafer fragment in process is indicated in Fig. 1 with reference numeral 10. Such comprises a bulk semiconductive substrate 12 which supports field oxide regions 14 and a gate oxide layer 16. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A gate structure 18 is formed proximate gate oxide 16, such as in an overlapping relationship. A top gated construction is shown,

although bottom gated constructions could also be utilized. Gate construction 18 is comprised of a first conductive material portion 20 (i.e., conductively doped polysilicon), and a higher conductive layer 22 (i.e., a silicide such as WSi_x). An insulating cap 24 is provided over layer 22, with SiO_2 and Si_3N_4 being example materials. For purposes of the continuing discussion, gate construction 18 defines opposing gate edges 26 and 28, and a center 30 therebetween. The invention is believed to have its greatest impact where the gate width between edges 26 and 28 (i.e., the channel length) is 0.25 micron or less.

Chlorine is provided within gate oxide layer 16 as indicated in the figure by the hash marks, and thus between semiconductive material of substrate 12 and transistor gate 18. Chlorine can be provided before or after formation of gate construction 18. For example, the chlorine in layer 16 can be provided by gas diffusion, ion implantation or *in situ* as initially deposited or formed. Preferred dopant concentration of the chlorine within oxide layer 16 is from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3. A source, a drain, and insulating sidewall spacers over gate construction 18 can be provided. Chlorine based gate oxides can improve hot-carrier immunity. The chlorine present at the Si/SiO_2 interface reduces the number of strained Si/O bonds, as fewer sites are available for defect formation. Improvements at the Si/SiO_2 interface will reduce junction leakage, the probability of charge trapping and interface state generation, thus improving device characteristics.

A second embodiment is described with reference to Figs. 2 and 3. Like numerals from the first described embodiment are utilized when appropriate, with differences being indicated by the suffix "b" or with different numerals. Wafer fragment 10b ideally comprises a gate oxide layer 16b which is initially provided to be essentially undoped with chlorine. The Fig. 2 construction is subjected to angle ion implanting (depicted with arrows 32) to implant at least one of chlorine or fluorine into gate oxide layer 16b beneath edges 26 and 28 of gate 18. A preferred angle for the implant is between from about 0.5° to about 10° from perpendicular to gate oxide layer 16b. An example energy range is from 20 to 50 keV, with 50 keV being a preferred example. An example implant species is SiF_3, to provide a fluorine dose of from about 1×10^{15} atoms/cm^2 to about 3×1^{15} atoms/cm^2, with 2×10^{15} atoms/cm^2 being a specific example. The resultant preferred implanted dopant concentration within layer 16b is from about 1×10^{19} atom/cm^3 to about 1×10^{21} atoms/cm^3.

The concentrated regions from such preferred processing will extend inwardly within gate oxide layer 16b relative to gate edges 26 and 28 a preferred distance of from about 50 Angstroms to about 500 Angstroms. Such is exemplified in the Figures by boundaries 34. In the physical product, such boundaries would not physically exist, but rather the implant concentration would preferably appreciably drop off over a very short distance of the channel length.

Annealing is preferably subsequently conducted to repair damage to the gate oxide layer caused by the ion implantation. Example conditions include exposure of the substrate to a temperature of from 700℃ to 1000℃ in an inert atmosphere such as N_2 at a pressure from 100 mTorr - 760 Torr for from about 20 minutes to 1 hour. Such can be conducted as a dedicated anneal, or in conjunction with other wafer processing whereby such conditions are provided. Such will also have the effect of causing encroachment or diffusion of the implanted atoms to provide barriers 34 to extend inwardly from edges 26 and 28 approximately from about 50 Angstroms to about 500 Angstroms.

Such provides but one example of doping and concentrating at least one of chlorine or fluorine in the gate oxide layer within the overlap region between the semiconductive material and the gate more proximate the gate edges 26 and 28 than gate center 30. Such preferably provides a pair of spaced and opposed concentration regions in the gate oxide layer, with the area between the concentration regions being substantially undoped with chlorine and fluorine. In the context of this document, "substantially undoped" and "substantially void" means having a concentration range of less than or equal to about 1×10^{16} atoms/cm^3.

Referring to Fig. 3, subsequent processing is illustrated whereby insulative sidewall spacers 36 are formed over the gate edges. A source region 38 and a drain region 40, as well as LDD regions 42, are provided.

The Figs. 2-3 embodiment illustrated exemplary provision of concentrated regions more proximate the gate edges by angle ion implanting and subsequent anneal. Alternate processing is described with other embodiments with reference to Figs. 4-10. A first alternate embodiment is shown in Figs. 4-6, with like numerals from the first described embodiment being utilized where appropriate, with differences being indicated with the suffix "c" or with different numerals.

Wafer fragment 10c is shown at a processing step subsequent to that depicted by Fig. 1 (however preferably with no chlorine provided in the gate oxide layer). The gate oxide material of layer 16c is etched substantially selective relative to silicon to remove oxide thereover, as shown. A layer of oxide to be used for spacer formation is thereafter deposited over substrate 12 and gate construction 18c. Such is anisotropically etched to form insulative sidewall spacers 44 proximate opposing lateral edges 26 and 28 of gate 18. Preferably as shown, such spacers are formed to cover less than all of the conductive material of lateral edges 26 and 28 of gate 18. Further in this depicted embodiment, such spacers 44 do not overlie any gate oxide material over substrate 12, as such has been completed etched away.

Spacers 44 are provided to be doped with at least one of chlorine or fluorine, with an example dopant concentration being 1×10^{21} atoms/cm^3. Such doping could be provided in any of a number of ways. For example, the deposited insulating layer from which spacers 44 are formed, for example SiO_2, could be *in situ* doped

during its formation to provide the desired fluorine and/or chlorine concentration. Alternately, such could be gas diffusion doped after formation of such layer, either before or after the anisotropic etch to form the spacers. Further alternately, and by way of example only, ion implanting could be conducted to provide a desired dopant concentration within spacers 44.

Referring to Fig. 5, spacers 44 are annealed at a temperature and for a time period effective to diffuse the dopant fluorine or chlorine from such spacers into gate oxide layer 16c beneath gate 18. Sample annealing conditions are as described above with respect to repair of ion implantation damage. Such can be conducted as a dedicated anneal, or as a byproduct of subsequent wafer processing wherein such conditions are inherently provided. Such provides the illustrated concentration regions 46 proximate lateral edges 26 and 28 with gate oxide material therebetween preferably being substantially undoped with either chlorine or fluorine.

Referring to Fig. 6, another layer of insulating material (i.e., silicon nitride or silicon dioxide) is deposited over gate 18 and sidewall spacers 44. Such is anisotropically etched to form spacers 48 about spacers 44 and gate construction 18. Preferably, such spacer 48 formation occurs after annealing to cause effective diffusion doping from spacers 44 into gate oxide layer 16c.

Alternate processing with respect to Fig. 5 is shown in Fig. 7. Like numerals from the first described embodiment are utilized where

appropriate with differences being indicated with the suffix "d". Here in a wafer fragment 10d, doped spacers 44 have been stripped from the substrate prior to provision of spacers 48. Accordingly, diffusion doping of chlorine or fluorine from spacers 44 would be conducted prior to such stripping in this embodiment. The Fig. 7 processing is believed to be preferred to that of Fig. 6, such that the chlorine or fluorine dopant atoms won't have any adverse effect on later or other processing steps in ultimate device operation or fabrication. For example, chlorine and fluorine may not be desired in the preferred polysilicon material of the gate.

A next alternate embodiment is described with reference to Figs. 8 and 9. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated with the suffix "e" or with different numerals. Fig. 8 illustrates a wafer fragment 10e which is similar to that depicted by Fig. 4 with the exception that gate oxide layer 16e has not been stripped or etched laterally outward of gate edges 26 and 28 prior to spacer 44e formation. Accordingly in such embodiment, spacers 44e are formed to overlie gate oxide layer 16e.

Referring to Fig. 9, such spacers are subjected to appropriate annealing conditions as described above to cause diffusion doping of the chlorine or fluorine into the gate oxide layer 16e and beneath gate 18 from laterally outward of gate edges 26 and 28. This embodiment is not believed to be as preferred as those depicted by Figs. 4-7, in that

the dopant must diffuse both initially downwardly into gate oxide layer 16 and then laterally to beneath gate edges 26 and 28.

Yet another alternate embodiment is described with reference to Fig. 10. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated with the suffix "f". Fig. 10 is similar to the Figs. 8-9 embodiment. However, gate oxide layer 16f is etched only partially into laterally outward of gate edges 26 and 28, thus reducing its thickness. Chlorine and/or fluorine doped spacers 44f are subsequently formed as described above. A diffusion annealing is then conducted. In comparison to the Fig. 8 embodiment, the Fig. 10 embodiment provides a portion of gate oxide layer 16f to be laterally outwardly exposed, such that dopant diffusion to beneath gate edges 26 and 28 is facilitated.

Provision of fluorine and/or chlorine at the edges, with a central region therebetween being substantially void of same, reduces or eliminates any adverse affect chlorine and/or fluorine would have at the center of the gate where hot electron carrier effects are not as prominent.

The above-described embodiments preferably place doped chlorine or fluorine proximate both gate edges 26 and 28 within the respective gate oxide layers. Alternately, such greater concentration could be provided proximate only one of the gate edges, such as the drain edge where the hot carrier effects are most problematic.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming a transistor gate comprising:

forming a gate oxide layer over a semiconductive substrate;

providing chlorine within the gate oxide layer; and

forming a gate proximate the gate oxide layer.

2. The method of claim 1 wherein the chlorine is provided after forming the gate.

3. The method of claim 1 wherein the chlorine is provided before forming the gate.

4. The method of claim 1 wherein the chlorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

5. The method of claim 1 wherein the gate comprises opposing lateral edges and a central region therebetween, the chlorine being provided within the gate oxide layer to a greater concentration proximate at least one of the gate edges than in the central region.

6. A method of forming a transistor gate comprising:

forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a center therebetween; and

concentrating at least one of chlorine or fluorine in the gate oxide layer within the overlap more proximate at least one of the gate edges than the center.

7. The method of claim 6 wherein the concentrating comprises concentrating fluorine.

8. The method of claim 6 wherein the gate is formed to have a gate width between the edges of 0.25 micron or less, the concentrating forming at least one concentration region in the gate oxide which extends laterally inward from the at least one gate edge no more than about 500 Angstroms.

9. The method of claim 6 wherein the concentrating comprises diffusion doping.

10. The method of claim 6 wherein the concentrating comprises ion implanting.

11. A method of forming a transistor gate comprising:

forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a central region therebetween; and

doping the gate oxide layer within the overlap with at least one of chlorine or fluorine proximate the opposing gate edges and leaving the central region substantially undoped with chlorine and fluorine.

12. The method of claim 11 wherein the doping comprises ion implanting.

13. The method of claim 11 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

14. A method of forming a transistor gate comprising the following sequential steps:

forming a gate over a gate oxide layer, the gate having opposing edges; and

angle ion implanting at least one of chlorine or fluorine into the gate oxide layer beneath the edges of the gate.

15. The method of claim 14 wherein the angle is between from about 0.5 degrees to about 10 degrees from perpendicular the gate oxide layer.

16. The method of claim 14 further comprising annealing the gate oxide layer after the implanting.

17. A method of forming a transistor gate comprising the following sequential steps:

forming a gate over a gate oxide layer, the gate having opposing lateral edges; and

diffusion doping at least one of chlorine or fluorine into the gate oxide layer beneath the gate from laterally outward of the gate edges.

18. The method of claim 17 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

19. The method of claim 17 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms.

20. The method of claim 17 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms, the concentration regions having an average dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

21. The method of claim 20 wherein the gate oxide layer between the concentration regions is substantially undoped with chlorine and fluorine.

22. A method of forming a transistor gate comprising the following steps:

forming a gate over a gate oxide layer, the gate having opposing lateral edges;

forming sidewall spacers proximate the opposing lateral edges, the sidewall spacers comprising at least one of chlorine or fluorine; and

annealing the spacers at a temperature and for a time period effective to diffuse the fluorine or chlorine from the spacers into the gate oxide layer to beneath the gate.

23. The method of claim 22 wherein after the annealing, stripping the spacers from the edges.

24. The method of claim 22 comprising forming the spacers to cover less than all of the lateral edges.

25. The method of claim 22 comprising forming the spacers to overlie the gate oxide layer.

26. The method of claim 22 comprising forming the spacers to not overlie any of the gate oxide layer.

27. The method of claim 22 further comprising:

depositing a layer of insulating material over the gate and the sidewall spacers; and

anisotropically etching the layer of insulating material to form spacers over the sidewall spacers.

28. The method of claim 27 wherein the annealing occurs before the depositing.

29. The method of claim 27 wherein the annealing occurs after the depositing.

30. The method of claim 22 further comprising:

providing gate oxide layer material laterally outward of the gate edges;

etching only partially into the gate oxide layer laterally outward of the gate edges; and

forming said sidewall spacers over the etched gate oxide layer laterally outward of the gate edges.

31. A transistor comprising:

a semiconductive material and a transistor gate having gate oxide positioned therebetween, the gate having opposing gate edges and a central region therebetween;

a source formed laterally proximate one of the gate edges and a drain formed laterally proximate the other of the gate edges; and

chlorine within the gate oxide layer between the semiconductive material and the transistor gate.

32. The transistor of claim 31 wherein the chlorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

33. The transistor of claim 31 wherein the chlorine is provided within the gate oxide layer to a greater concentration proximate at least one of the gate edges than in the central region.

34. The transistor of claim 31 wherein the chlorine is provided within the gate oxide layer to a greater concentration proximate the other gate edge than in the central region.

35. The transistor of claim 31 wherein the chlorine is provided within the gate oxide layer to a greater concentration proximate both gate edges than in the central region.

36. The transistor of claim 31 wherein the central region is substantially void of chlorine.

37. A transistor comprising:

a semiconductive material and a transistor gate having gate oxide positioned therebetween, the gate having opposing gate edges and a central region therebetween;

a source formed laterally proximate one of the gate edges and a drain formed laterally proximate the other of the gate edges; and

at least one of fluorine or chlorine being concentrated in the gate oxide layer between the semiconductive material and the transistor gate more proximate at least one of the gate edges than the central region.

38. The transistor of claim 37 wherein fluorine is concentrated.

39. The transistor of claim 37 wherein chlorine is concentrated.

40. The transistor of claim 37 wherein the central region of the gate oxide layer is substantially void of chlorine and fluorine.

41. The transistor of claim 37 wherein the concentrated chlorine or fluorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

42. The transistor of claim 37 wherein the concentrated chlorine or fluorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3, and wherein the central region of the gate oxide layer is substantially void of chlorine and fluorine.

43. The transistor of claim 37 wherein the at least one of fluorine or chlorine is concentrated in the gate oxide layer more proximate both gate edges than in the central region.

44. The transistor of claim 37 wherein the at least one of fluorine or chlorine is concentrated in the gate oxide layer more proximate at least the other gate edge.

45. The transistor of claim 37 wherein the gate is formed to have a gate width between the edges of 0.25 micron or less, the concentrated at least one of fluorine or chlorine extending laterally inward from the at least one gate edge no more than about 500 Angstroms.

46. The transistor of claim 37 wherein the gate is formed to have a gate width between the edges of 0.25 micron or less, the concentrated at least one of fluorine or chlorine extending laterally inward from the at least one gate edge no more than about 500 Angstroms with an average concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

47. A transistor comprising:

a semiconductive material and a transistor gate having gate oxide positioned therebetween, the gate having opposing gate edges;

a source formed laterally proximate one of the gate edges and a drain formed laterally proximate the other of the gate edges;

first insulative spacers formed proximate the gate edges, the first insulative spacers being doped with at least one of chlorine or fluorine; and

second insulative spacers formed over the first insulative spacers.

48. The transistor of claim 47 wherein the second insulative spacers at least as initially provided are substantially undoped with either chlorine or fluorine.

49. The transistor of claim 47 further comprising at least one of chlorine or fluorine within the gate oxide layer proximate the gate edges.

50. The transistor of claim 47 wherein the gate oxide layer includes a central region between the opposing gate edges, and further comprising at least one of chlorine or fluorine within the gate oxide layer proximate the gate edges, the central region being substantially void of chlorine and fluorine.

ABSTRACT OF THE DISCLOSURE

A method of forming a transistor gate includes forming a gate oxide layer over a semiconductive substrate. Chlorine is provided within the gate oxide layer. A gate is formed proximate the gate oxide layer. In another method, a gate and a gate oxide layer are formed in overlapping relation, with the gate having opposing edges and a center therebetween. At least one of chlorine or fluorine is concentrated in the gate oxide layer within the overlap more proximate at least one of the gate edges than the center. Preferably, the central region is substantially undoped with fluorine and chlorine. The chlorine and/or fluorine can be provided by forming sidewall spacers proximate the opposing lateral edges of the gate, with the sidewall spacers comprising at least one of chlorine or fluorine. The spacers are annealed at a temperature and for a time effective to diffuse the fluorine or chlorine into the gate oxide layer to beneath the gate. Transistors and transistor gates fabricated according to the above and other methods are disclosed. Further, a transistor includes a semiconductive material and a transistor gate having gate oxide positioned therebetween. A source is formed laterally proximate one of the gate edges and a drain is formed laterally proximate the other of the gate edges. First insulative spacers are formed proximate the gate edges, with the first insulative spacers being doped with at least one of chlorine or fluorine. Second insulative spacers formed over the first insulative spacers.

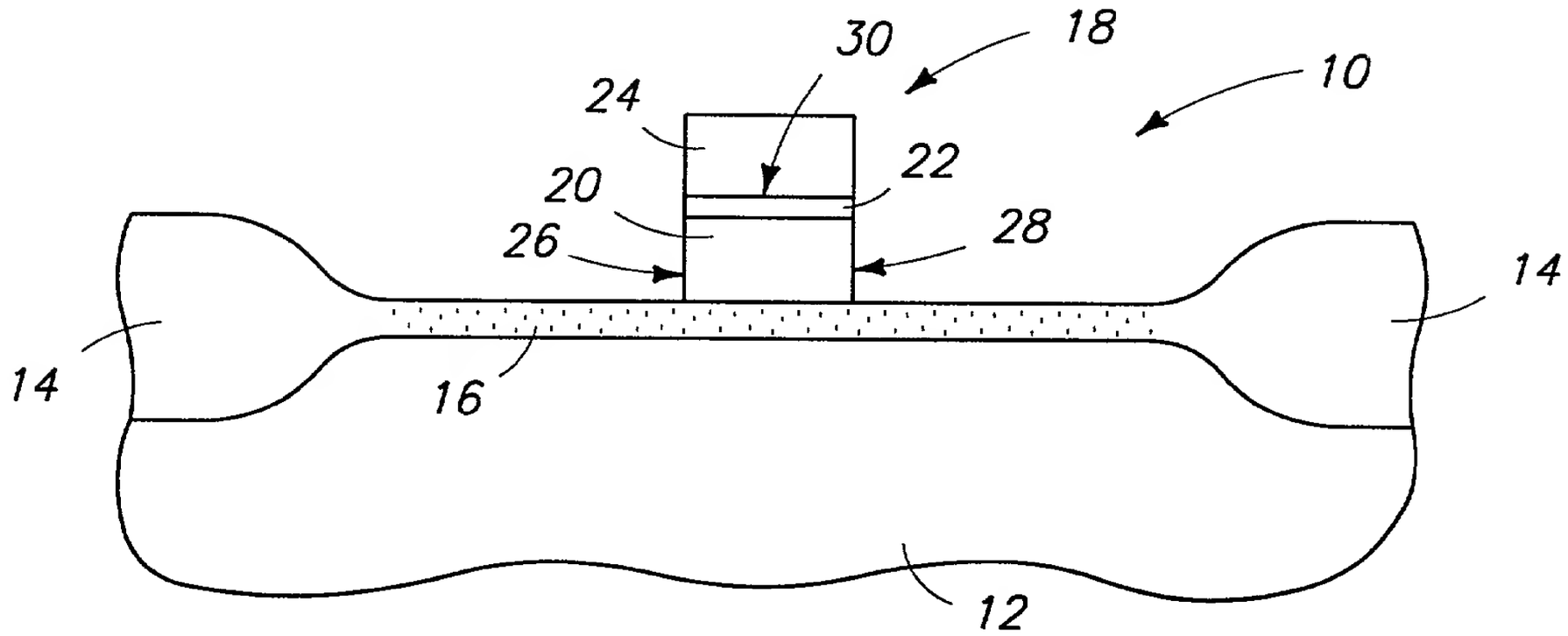


Fig. 1

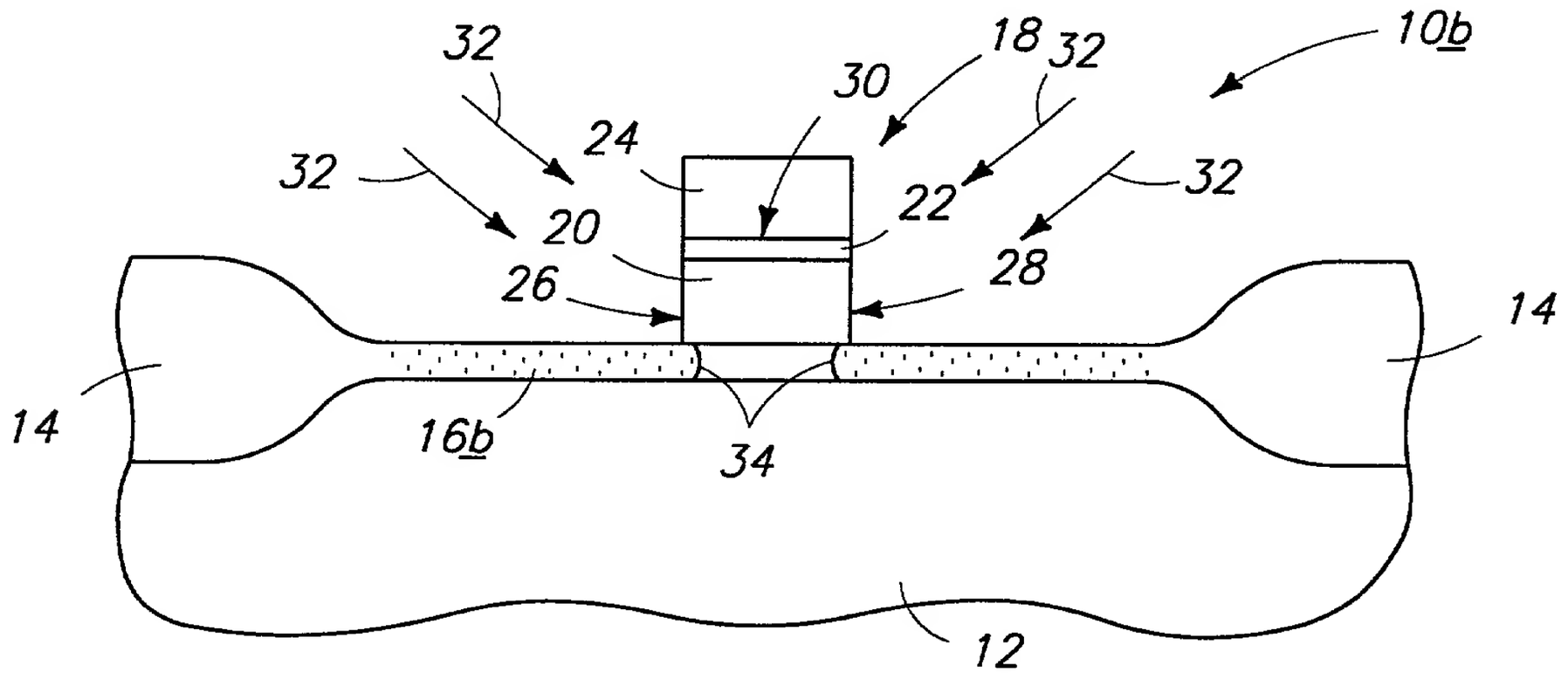


Fig. 2

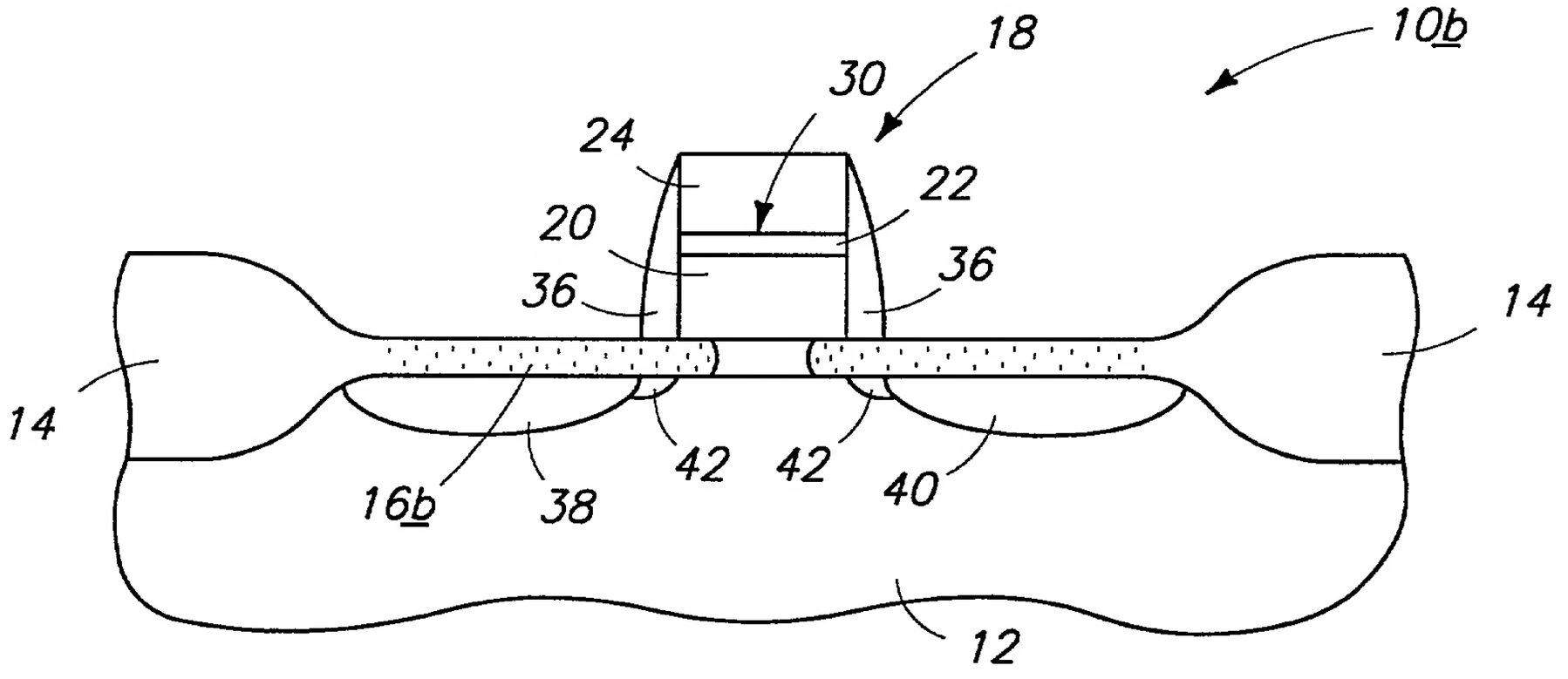


Fig. 3

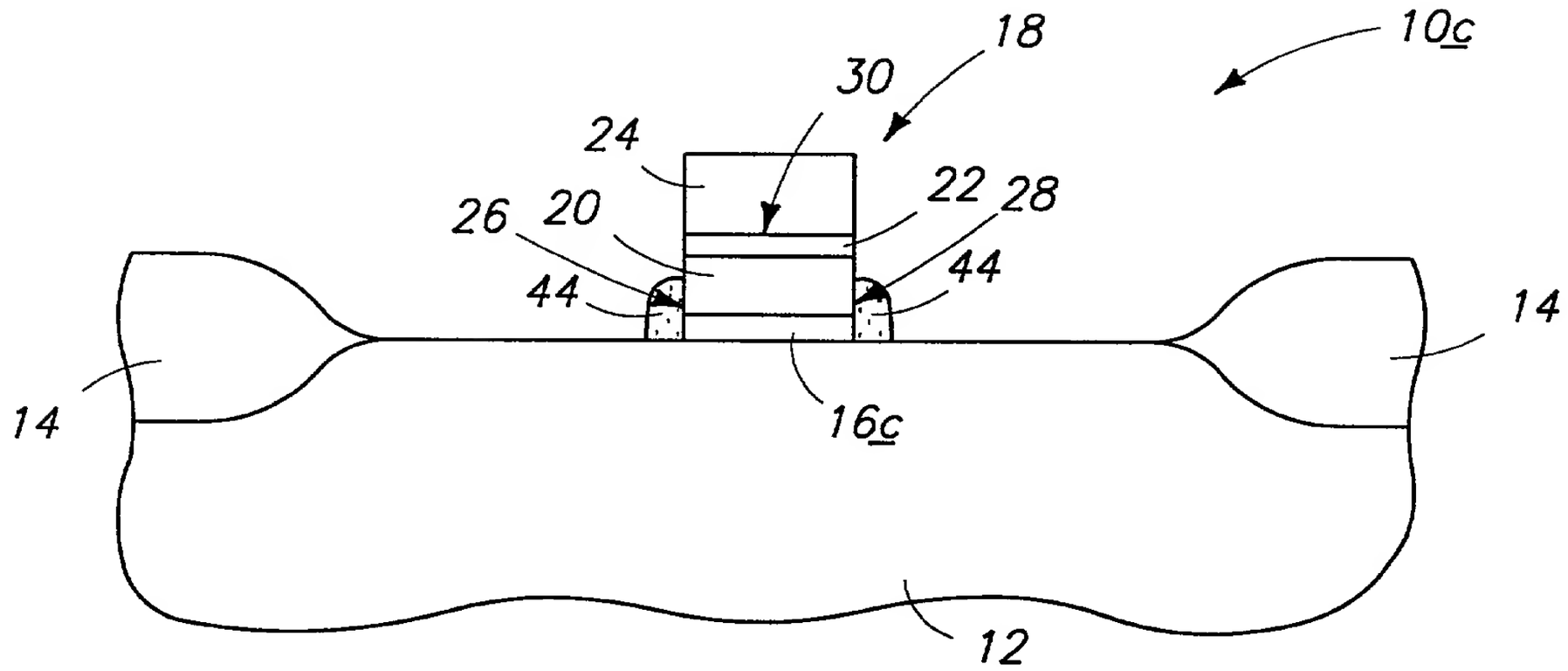


Fig 4

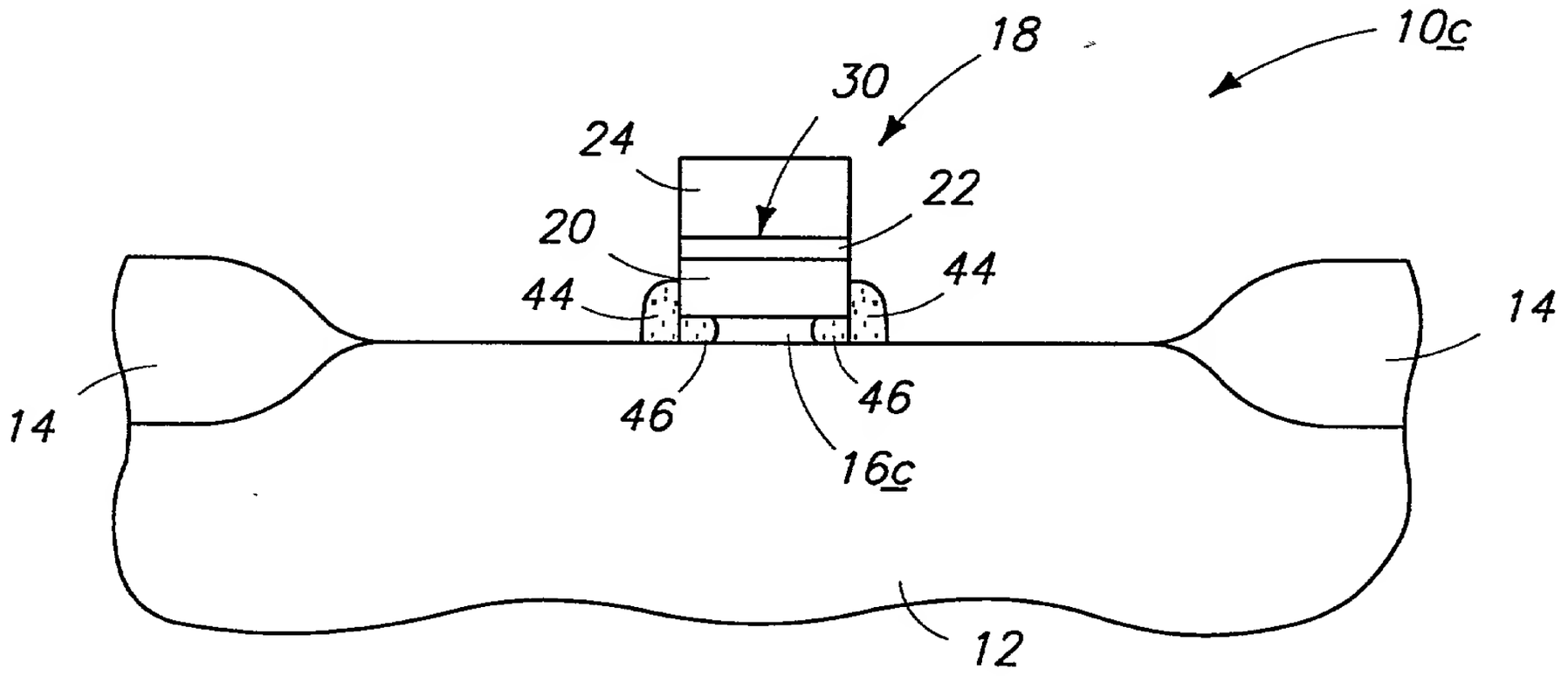


Fig 5

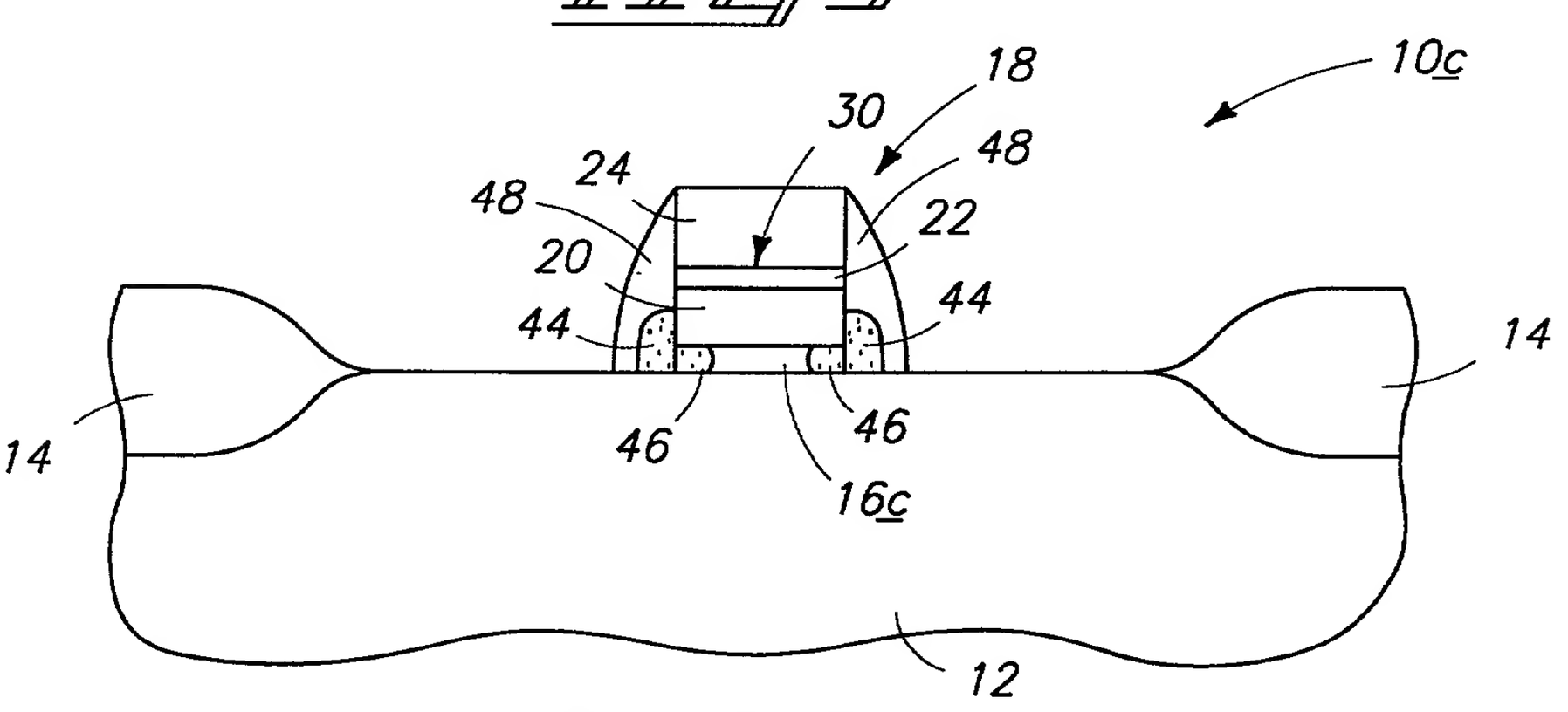
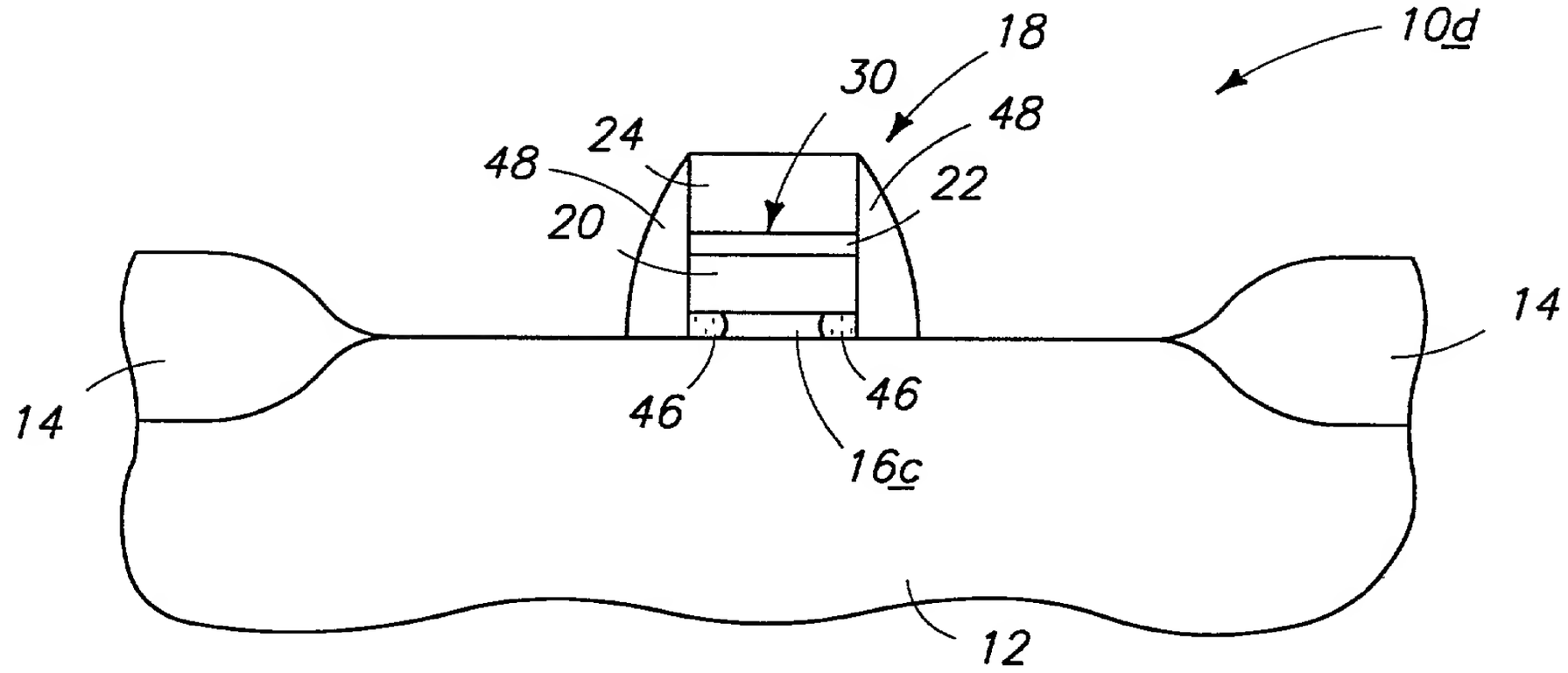


Fig 6


18
10d
30
24
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48
22
20
14
14
46
46
16c
12

Fig 7

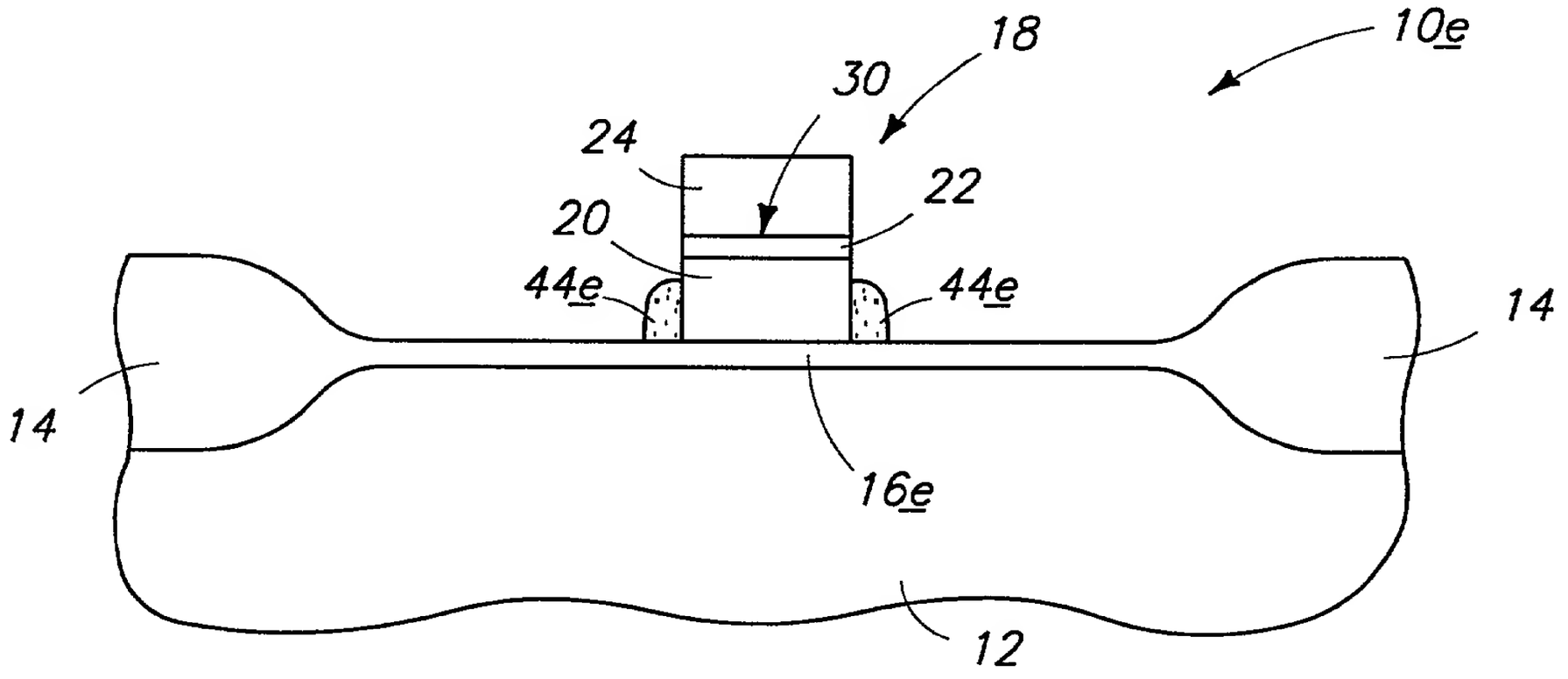
18
10e
30
24
22
20
44e
44e
14
14
16e
12

Fig 8

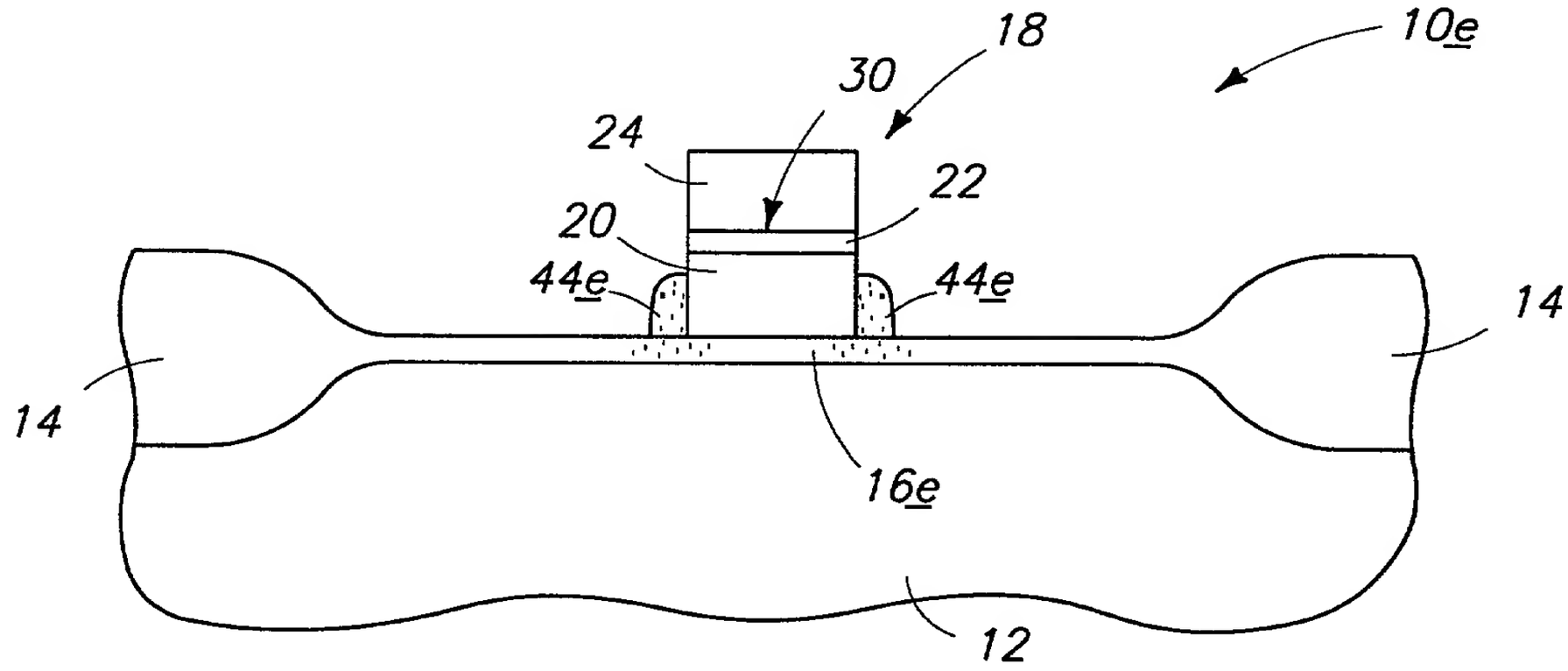

Fig 9

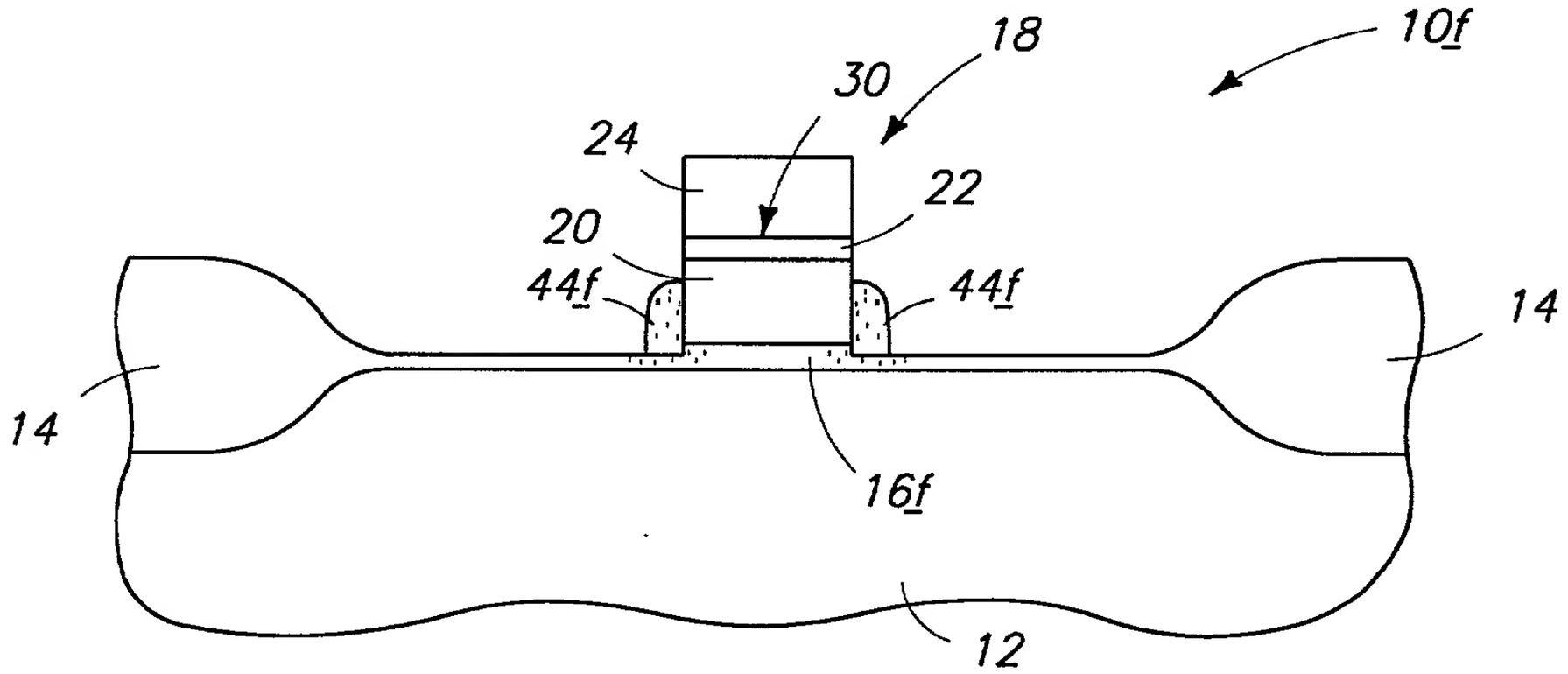

Fig 10

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Semiconductor Processing Method And Field Effect Transistor**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen,

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

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